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# fichier de configuration des pattes
# par Pierre Langlois
# v. 1.1, 2007/05/31 -- ajout de l'horloge et mise ‡ jour des affichages ‡ segments
# ----------------------------------------------------------------------------
# planchette Xilinx University Program Virtex-II Pro Development System

# horloge
#NET "clk" LOC = "AJ15"; # 100 MHz System Clock
# planchette d'expansion DIO4

# LEDs
#NET "ld<8>" LOC = "V6";
#NET "ld<7>" LOC = "U8";
#NET "ld<6>" LOC = "Y1";
#NET "ld<5>" LOC = "V4";
#NET "ld<4>" LOC = "U9";
#NET "ld<3>" LOC = "W2";
#NET "ld<2>" LOC = "U5";
#NET "ld<1>" LOC = "T8";

#NET "ldg" LOC = "V7";

# slide switches
#NET "sw<8>" LOC = "N4";
#NET "sw<7>" LOC = "P8";
#NET "sw<6>" LOC = "N1";
#NET "sw<5>" LOC = "M4";
#NET "sw<4>" LOC = "P9";
#NET "sw<3>" LOC = "M2";
#NET "sw<2>" LOC = "L5";
#NET "sw<1>" LOC = "N6";


# push buttons
#NET "pb<5>" LOC = "AA1";
#NET "pb<4>" LOC = "V8";
#NET "pb<3>" LOC = "W3";
#NET "pb<2>" LOC = "P2";
#NET "pb<1>" LOC = "P3";

# seven segment display (ssd) - shared segments - cathodes
#NET "ssd<7>" LOC = "N3"; #point
#NET "ssd<6>" LOC = "P7"; #g
#NET "ssd<5>" LOC = "P1"; #f
#NET "ssd<4>" LOC = "M3"; #e
#NET "ssd<3>" LOC = "R9"; #d
#NET "ssd<2>" LOC = "N2"; #c
#NET "ssd<1>" LOC = "L4"; #b
#NET "ssd<0>" LOC = "N5"; #a

# seven segment display - anodes (ssdan)
#NET "ssdan<0>" LOC = "W4";
#NET "ssdan<1>" LOC = "W5";
#NET "ssdan<2>" LOC = "AB1";
#NET "ssdan<3>" LOC = "Y4";
```